Expression of Interest for participating in the H2020 Innovation Pilot on detector technologies at accelerators

Title: *A versatile data acquisition system for silicon detectors based on programmable hardware*

Participants (max. 6): *list the participating institutes, laboratories and industrial partners*

Name of the legal entity	Type (university, institute, laboratory, company)	Country
CERN	Laboratory	CH
Geneva University (t.b.c.)	University	CH
HEPHY Vienna (t.b.c.)	Institute	AT
University of Liverpool (t.b.c.)	University	GB
IFIC Valencia (t.b.c.)	Institute	ES
Jožef Stefan Institute Ljubljana (t.b.c.)	Institute	SI

Contacts: *One name + e-mail per participant*

Participating institute / company	Main contact person	E-mail

Description: *(max. 1 page)*

Prototyping and testing of new silicon detectors requires the design of readout and control systems consisting of dedicated hardware and software for data acquisition. This task is time consuming and requires significant resources for each new detector prototype. This EOI aims at developing and supporting a common flexible readout platform, useable for different silicon detector projects within the AIDA++ consortium. The platform will initially be based on the Xilinx Zynq System-On-Chip architecture combining programmable hardware (FPGA) with a full Linux operating system giving access to high-level programming languages for readout software development. The FPGA controls a generic board with programmable power supplies, ADCs, clock and communication interfaces, which is connected to an application-specific chip board for signal routing to the detector. This modular hardware and software architecture allows for a cost-efficient and time-saving adaptation to various detector frontends, re-using components already developed for other detectors.

The activities proposed in this EOI concern on one hand the development and maintenance of the core system hardware architecture, support of new SoC platforms and additional Carboard features such as mezzanine SoC concepts. On the other hand, the partners will develop and share open-source FPGA-code and common readout software for the various projects. A version-control system and corresponding review procedures will be used to maintain a coherent and well-documented hardware architecture and code base.

It is expected that in the course of the project further participants from within the AIDA++ consortium and in the wider silicon-detector community will profit from and contribute to the open-source readout system. The proposed developments would also leverage strong synergies with the simulation and characterization activity in work package WP1 of the CERN EP R&D program.

Deliverables (max. 3): list the expected deliverable(s) of the proposed activities

- Production of common readout board
- Release of common readout firmware and software, validated with example use cases
- Comprehensive documentation of hardware and software

Budget estimate

- *Man-power (total number of person-months which are needed to achieve the objectives)*
- *Full cost including personnel and other direct costs (typically 1/3 EC contribution, 2/3 matching resources)*
- *DO NOT include overheads, which will be added to the EC contribution at the proposal preparation phase*

Total number of PMs	EC contribution (in kEUR) (a)	Matching funds (in kEUR) (b)	Full costs (in kEUR) (a) + (b)