

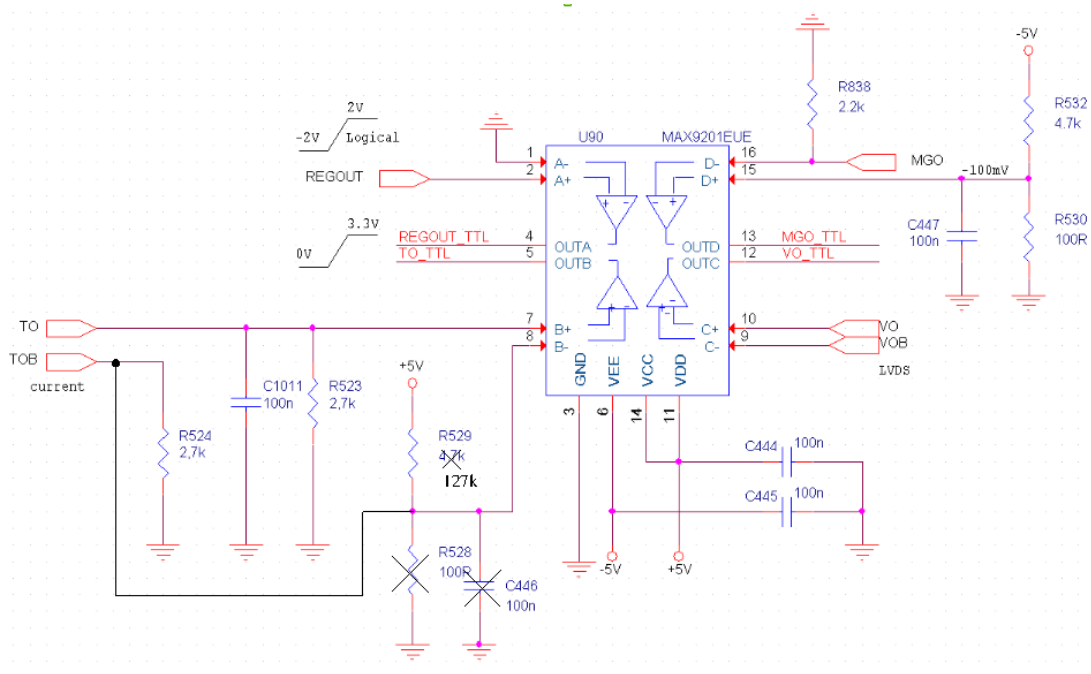
REPORT FROM VALENCIA 20th June 2013

Modifications in trigger line were done.

The ASIC's output is differential current type. This signal is terminated with resistors and passed through a comparator to obtain the desired levels.

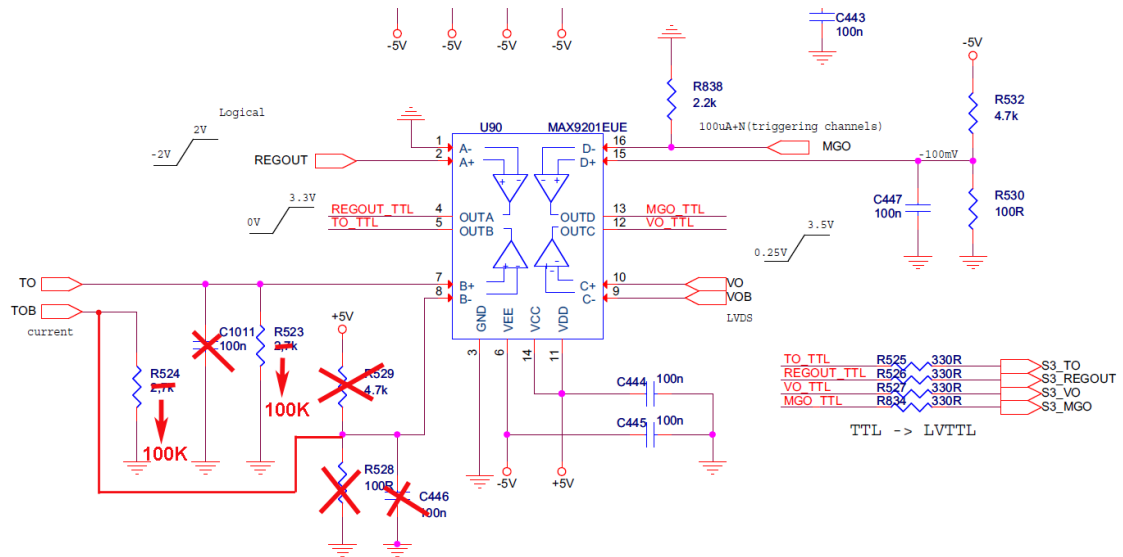
Andrej proposed a modification that solved problems with long cables. They were removing C446 and R528, connecting the negative part of the differential signal to the comparator and changing the value of R529 in order to keep the ratio of the voltage divider.

Please, take into account that C1011 is not mounted in the board from the beginning.



This circuit needs to wait until the signal crosses around 100mV in order to detect the level. This can take around 50 or 60 ns

I've modified this circuit achieving a delay of 4 ns. Changing the termination resistors increases the signal level improving the SNR.



This new circuit has been only tested with another VATA chip and has to be tested with GP7.

In the next meeting I will present the results for GP7.