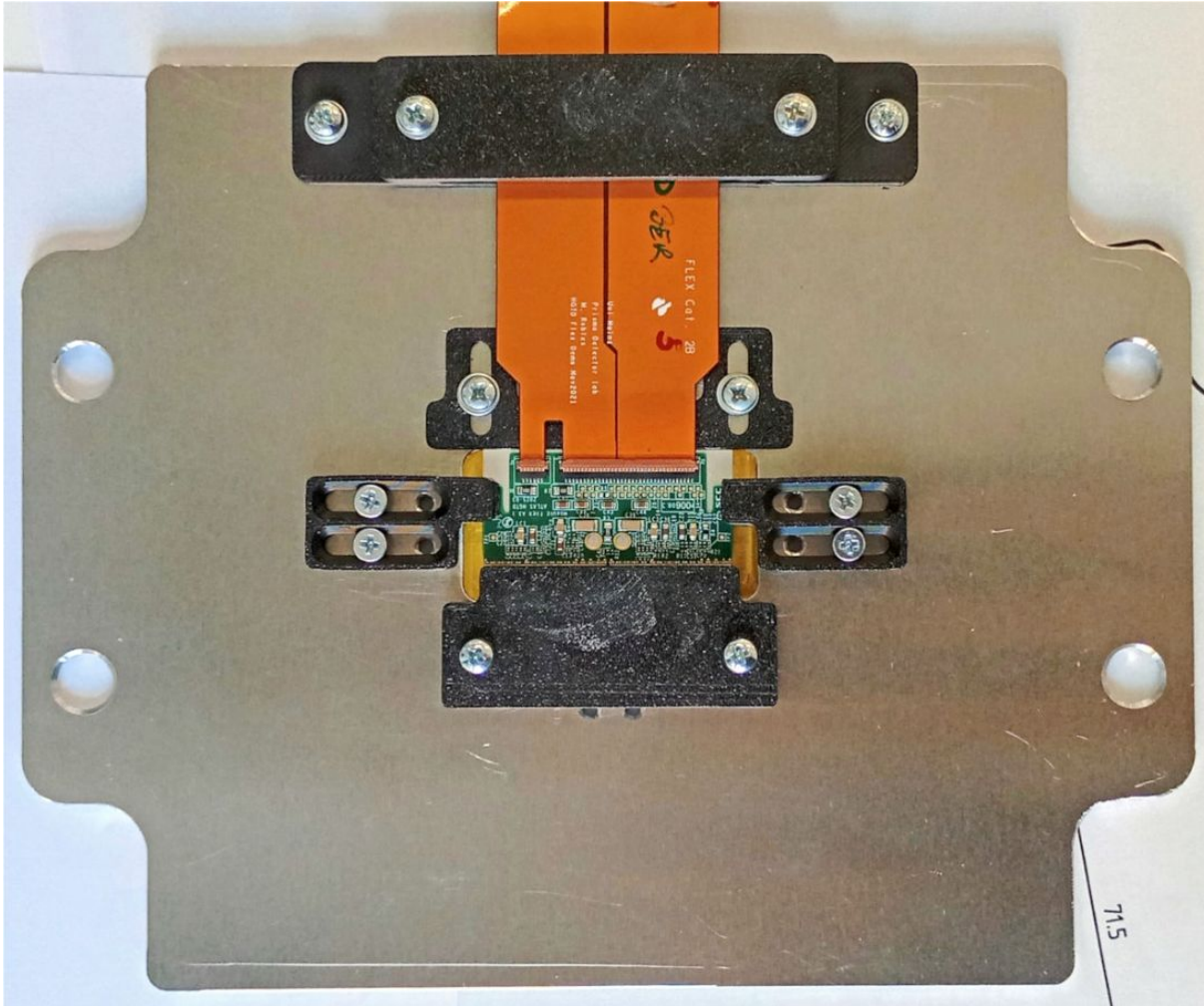
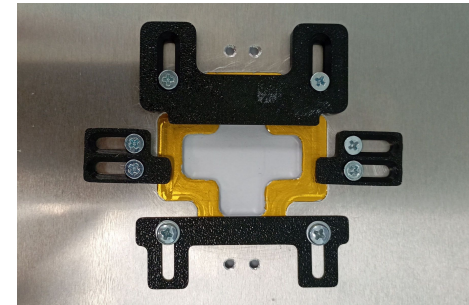


Module holder with module installed



First module successfully mounted on module holder

- Can communicate with device
- Both chips can be tuned to 4.8 fC
- Some noisy pixels
- Disconnected pads (already present from beginning, some new ones due to suboptimal handling)
- Could clamp design damage modules? (Already replaced tips with even softer rubber)
- Not enough support on the bottom?

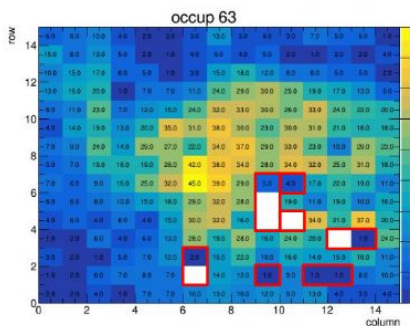


Module assembly info

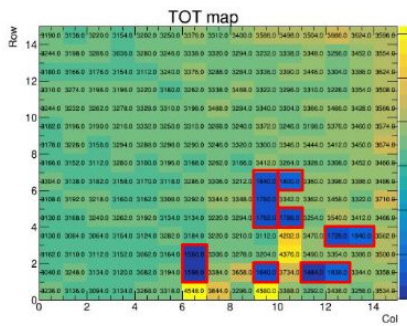
PP029

NCAP bumps, IFAE reflow

- Many disconnected pixels for chip 0, one for chip 1
- Analog scan (ToT map) seems even better than source scan



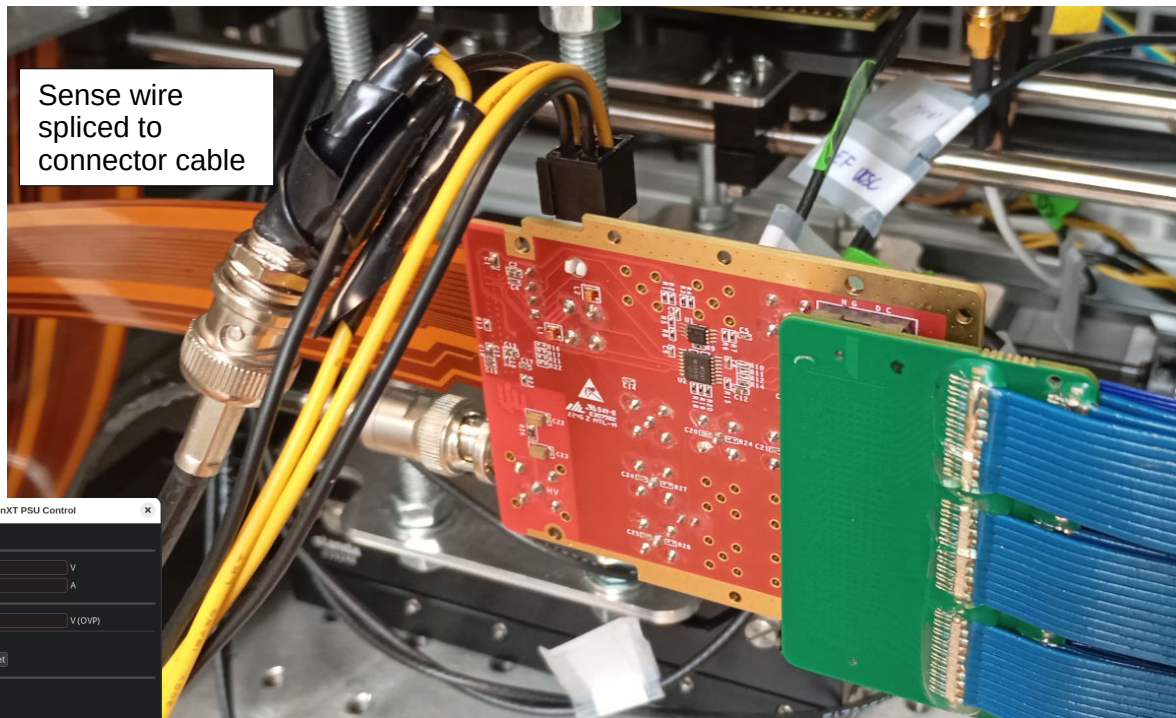
Sensor 0: IHEP 5-5 38



Sensor 1: IHEP 5-5 37

Powering modules

Replaced old power supply (Keithley 228A) with new 20 V 3 A linear supply (Sorensen XT 20-3)



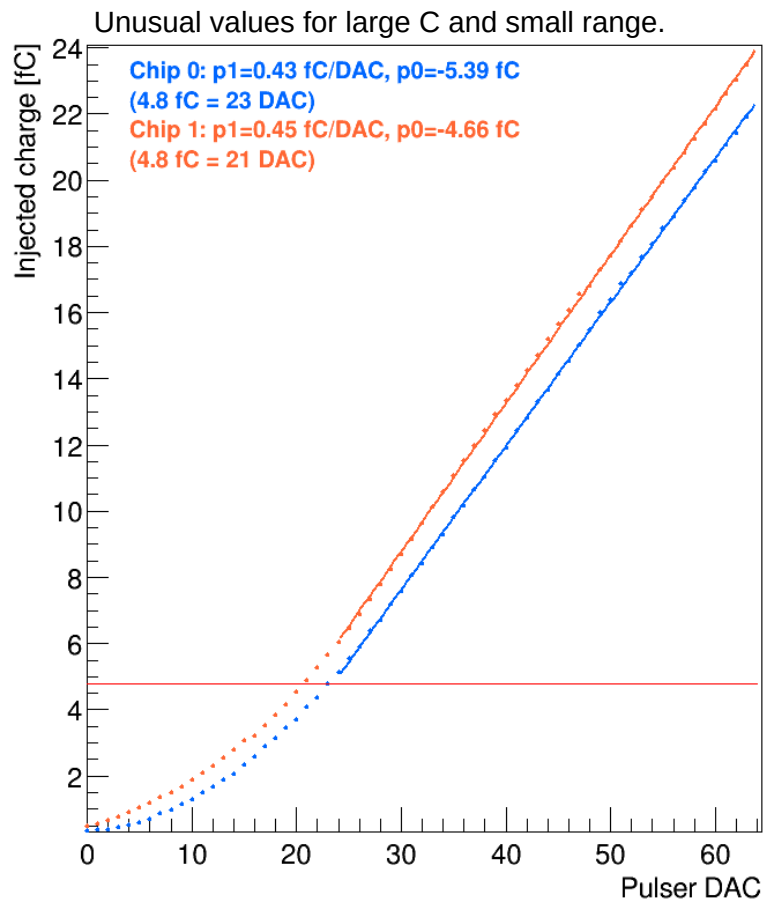
Control with GPIB (fixed one prologix interface board, trace was disconnected)

Soft turn ON/OFF, over voltage protection, use sense wires to compensate drop on supply cable (1.2 A at 1.34 V)

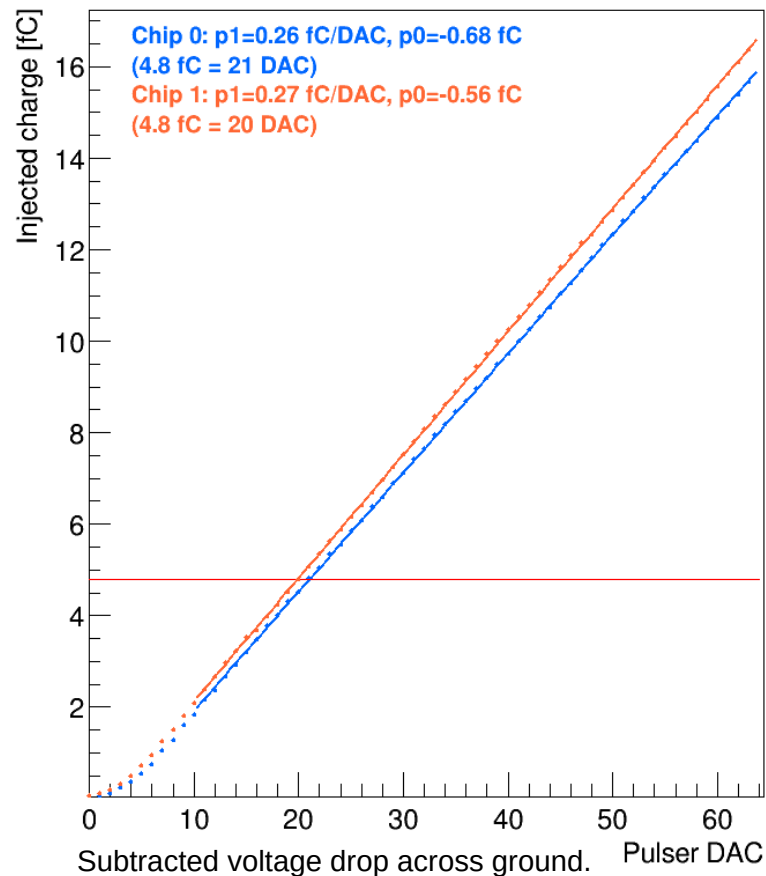
Some issues with power supply connector (resistance varies with amount of strain on cable)

Pulser calibration

Large C

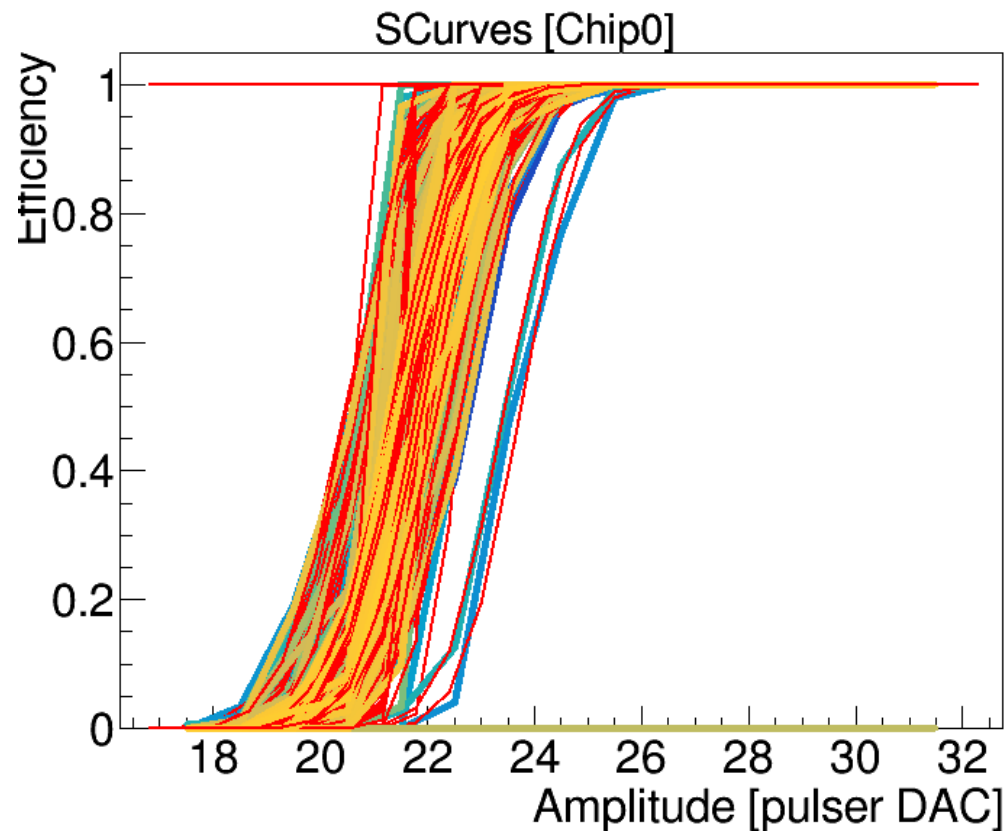
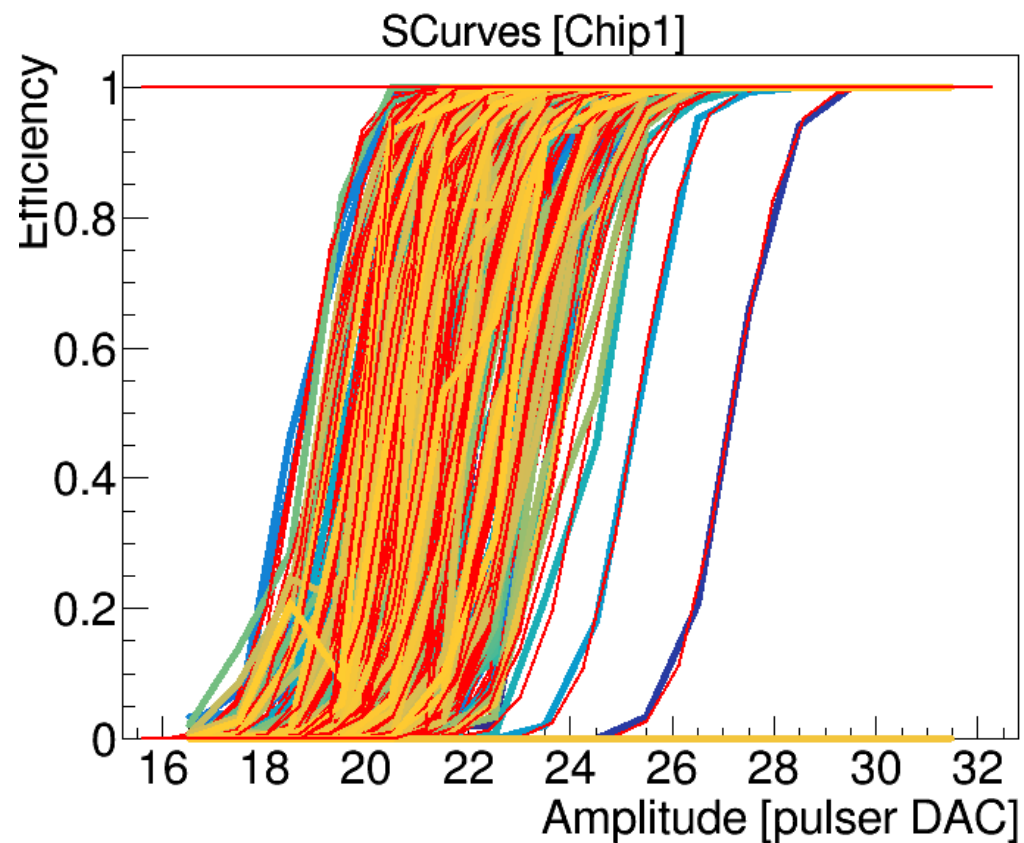


Small C



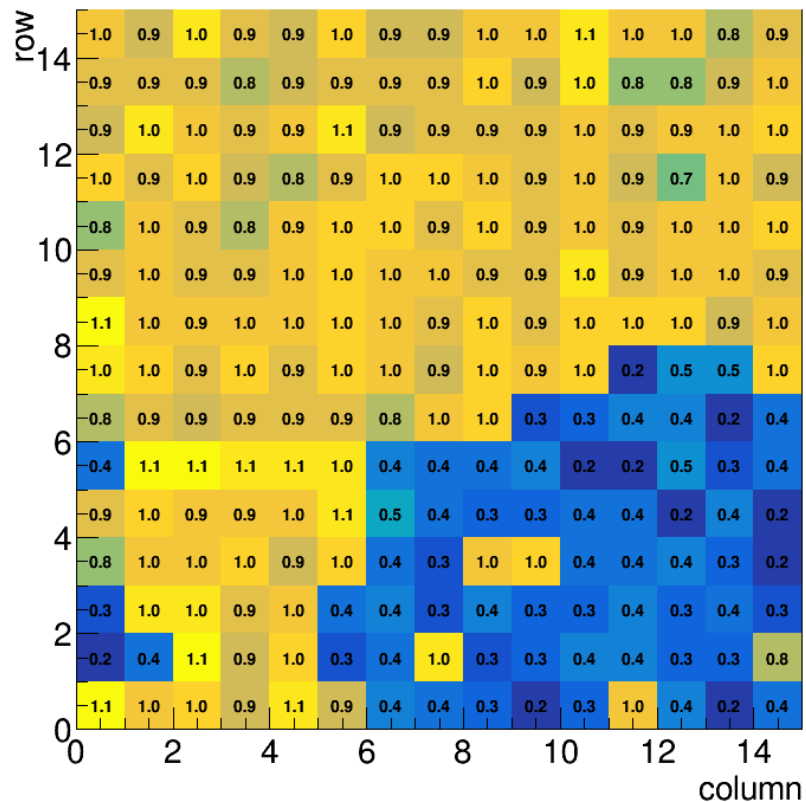
Tuning (4.8 fC)

$U_{HV} = 120 \text{ V}$, $I = 15.45 \text{ uA}$



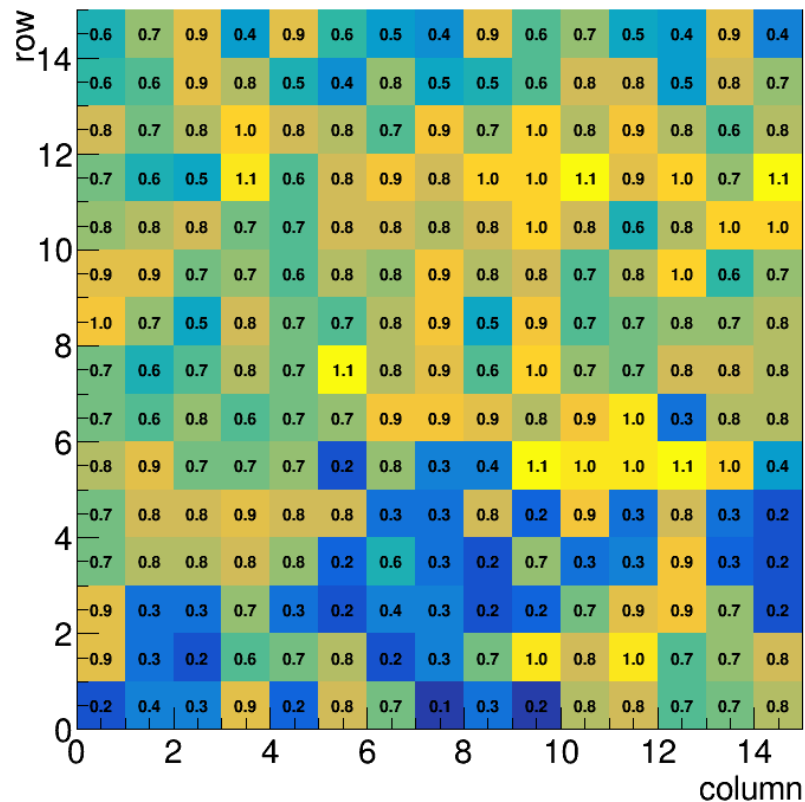
Noise

Noise (chip 0)



Many disconnected pads

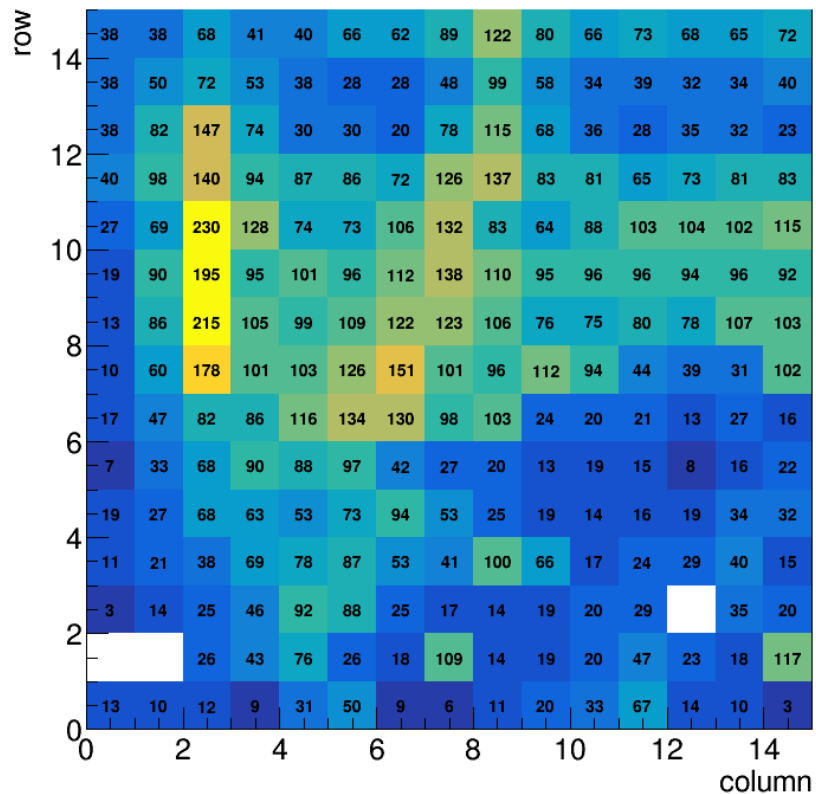
Noise (chip 1)



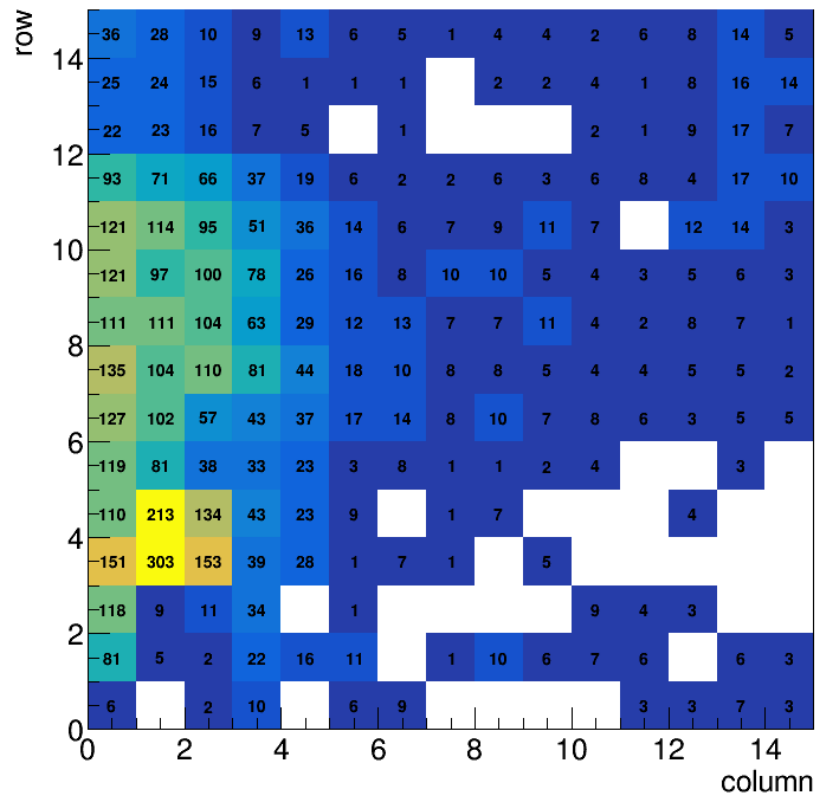
New disconnected pads (possible damage from transferring to holder?)

Flood image

Occupancy (chip 0)

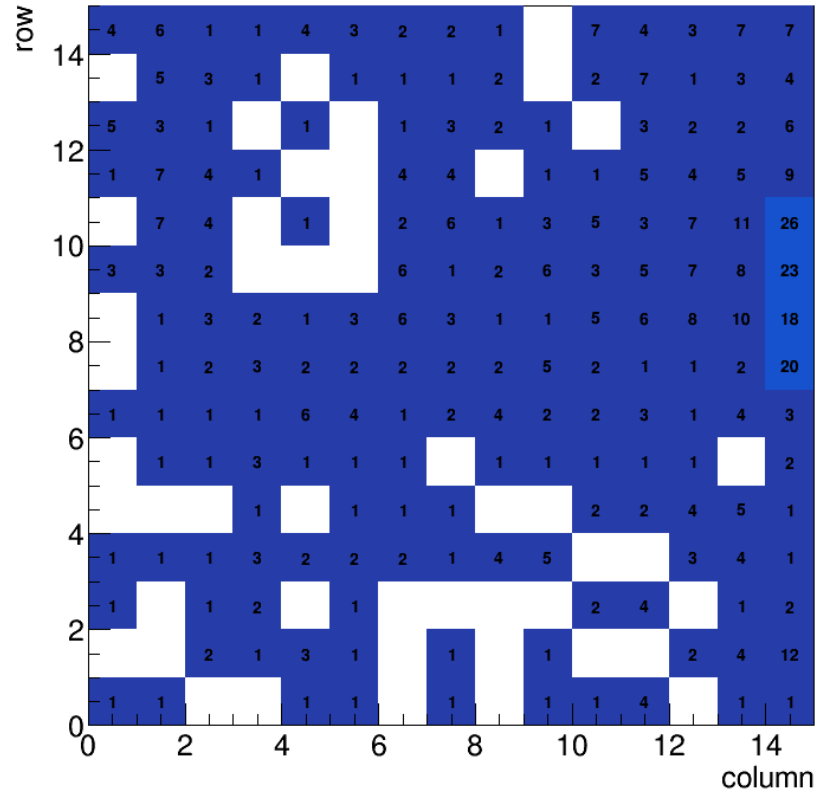


Occupancy (chip 1)

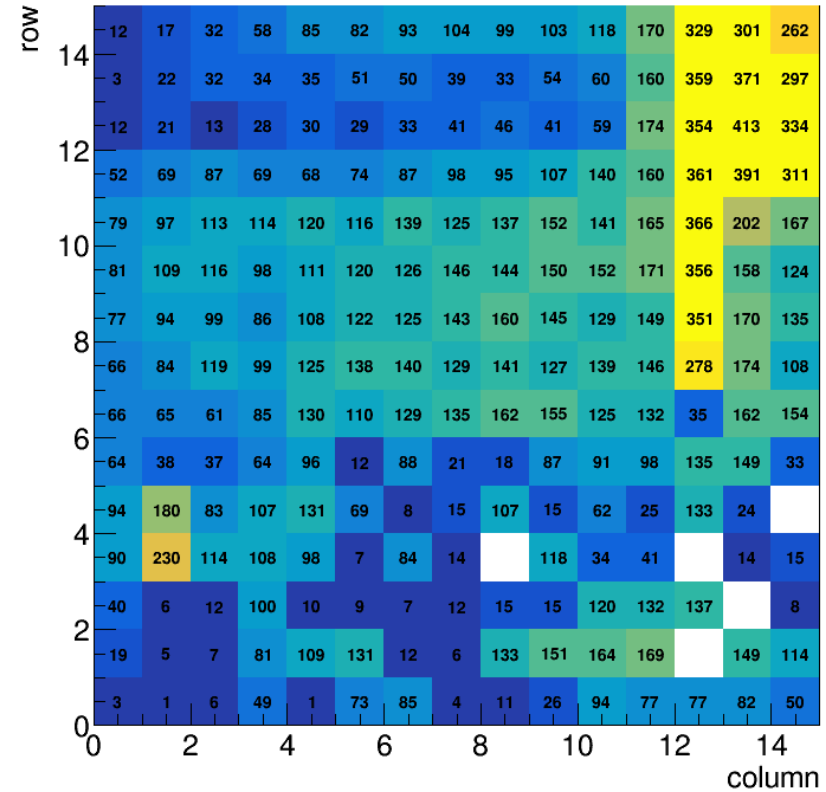


Flood image

Occupancy (chip 0)



Occupancy (chip 1)



Timing

- Work in progress, need to find a suitable reference clock
 - No convenient output available with current setup
 - Modules do not provide any clock output
 - Need additional hardware to get clock from FPGA?
 - All SMA ports on FPGA board are occupied (BUSY, TRIGGER)
 - One option is to use external clock generator (requires 320 MHz clock - differential signal, 2.5 V)
 - HP 8133A is usable (3 GHz max clock frequency, < 5 ps jitter)
 - Clock is injected in interface board -> goes to FPGA and then to ASICs
 - Need to use different firmware with external clock support