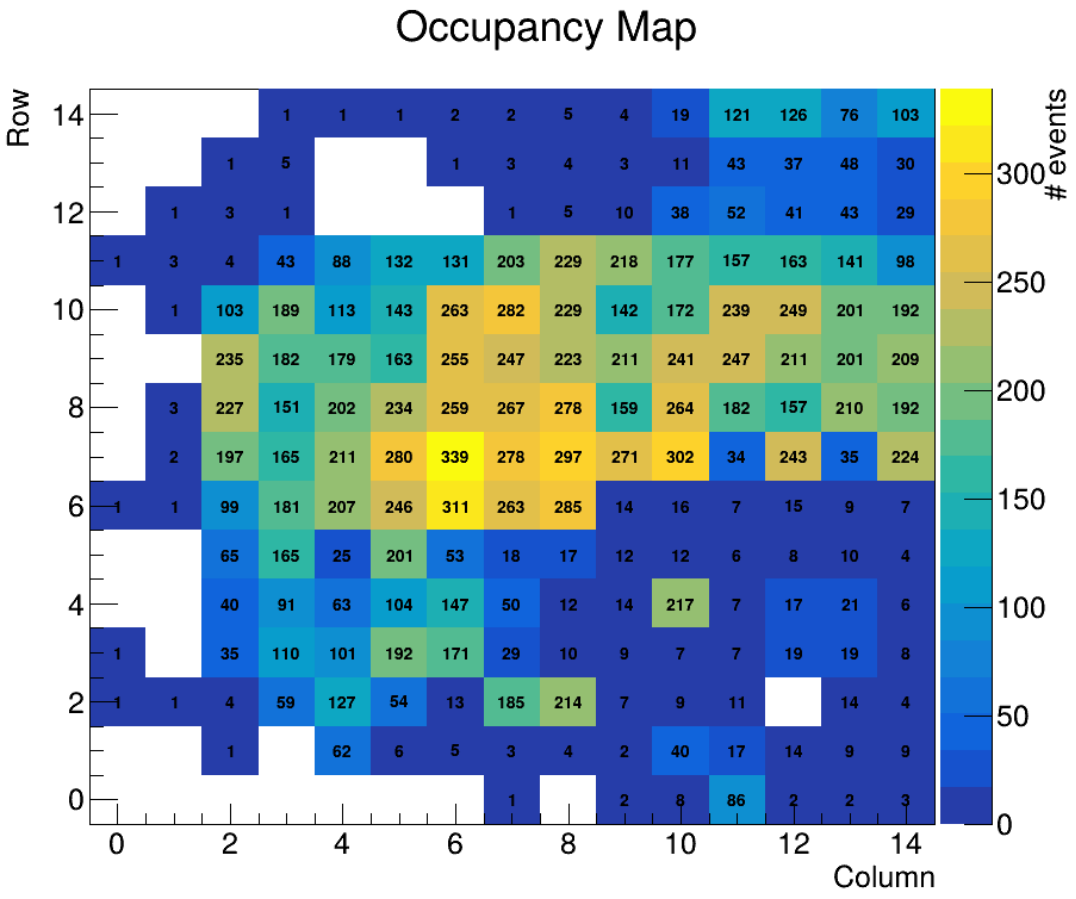
PP029 updates

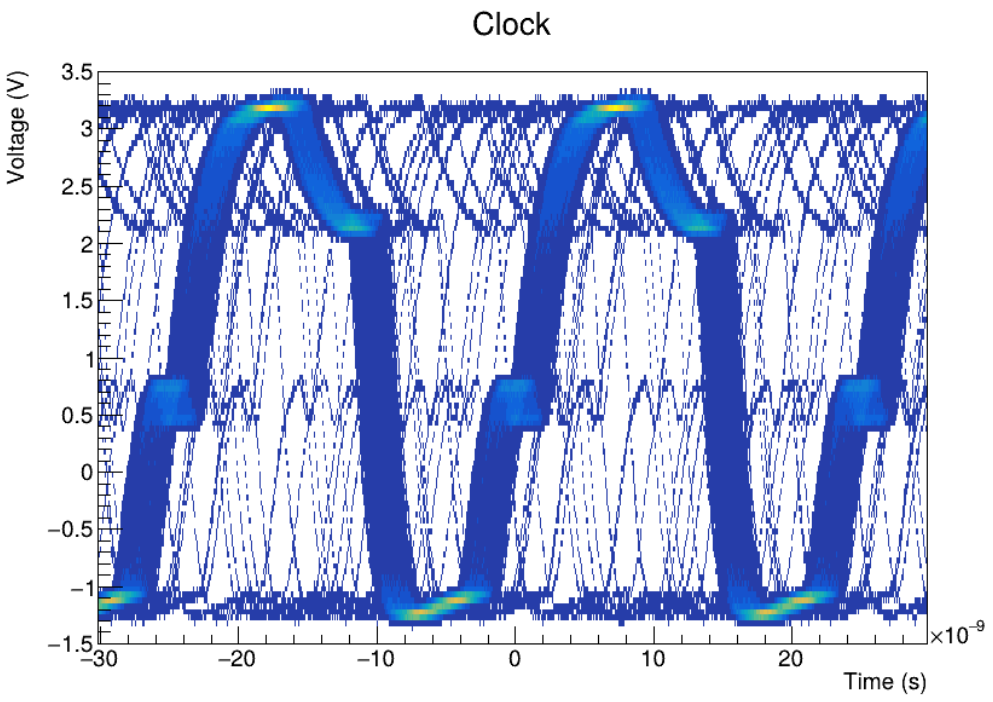


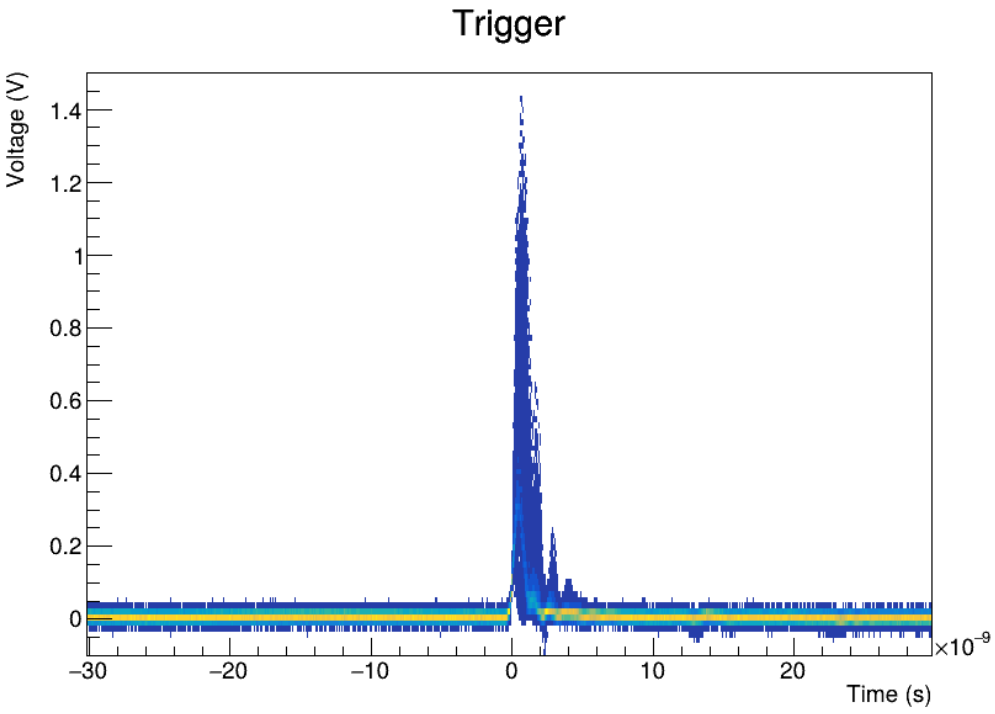
First data from module. As no clock is available directly from module firmware/software modification was required

- Stefano provided a way to output clock directly from FPGA
- This solution discards BUSY signal of FPGA, requiring some tweaks to acquisition process
- First data only from chip 0 as reading both requires some modification to readout software (almost complete)

Collected ~18k events overnight, have some issues with FPGA freezing - data taking randomly crashes after some time (4-6 hours). Similar issues in test beams, suggested fix is to run FPGA via direct ethernet connection to PC, but another NIC is required to do that.

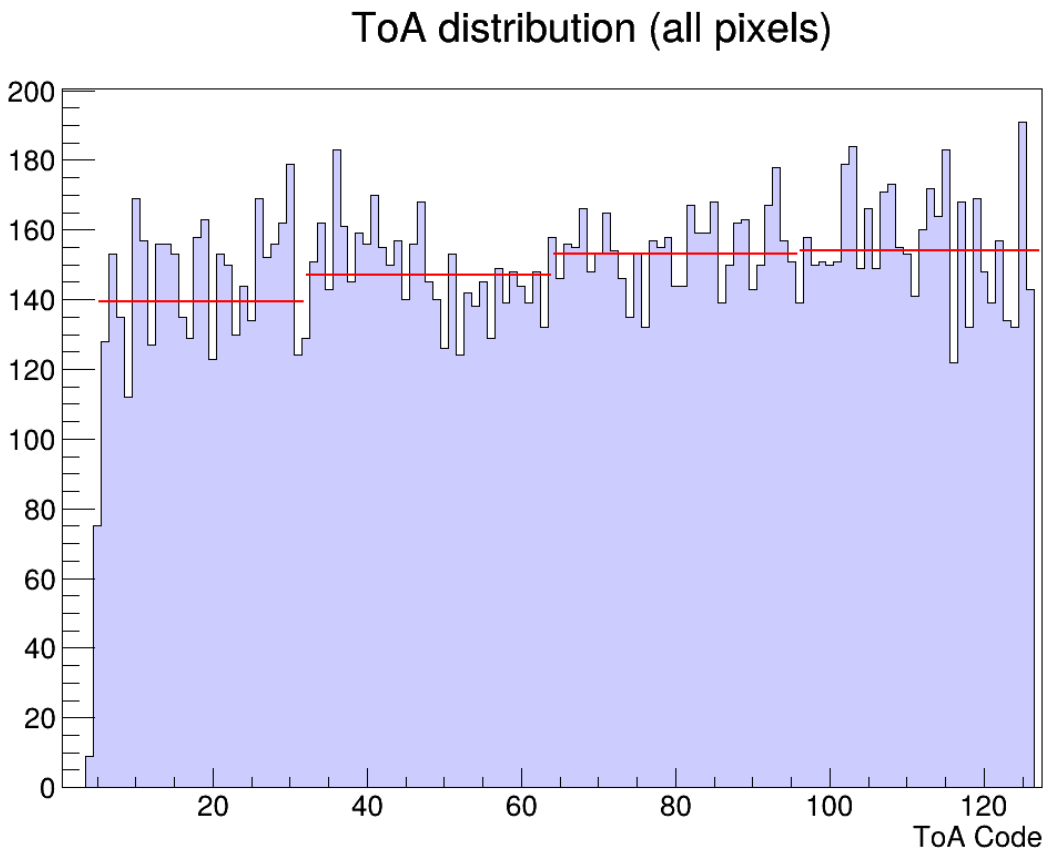
Clock and trigger signals





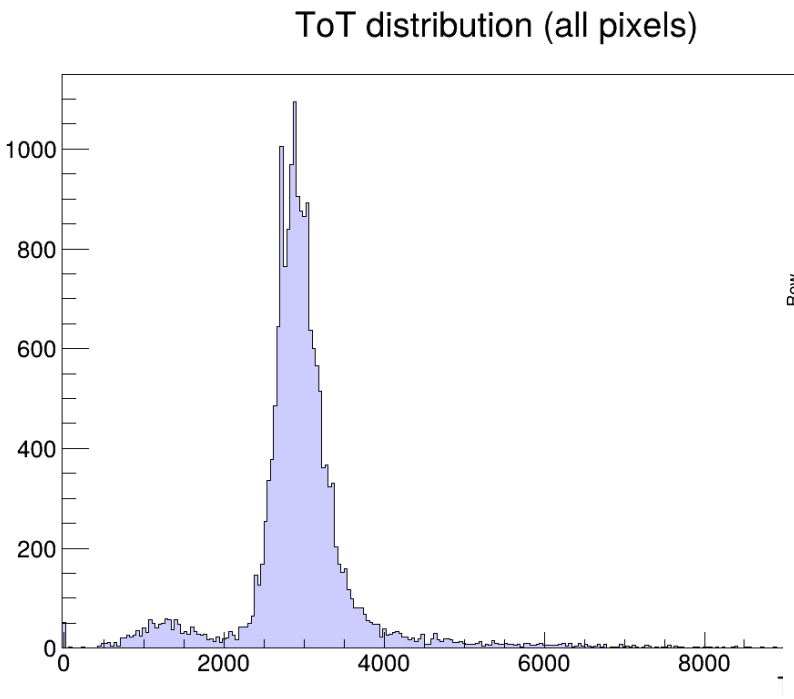
Timing acquisition with modified firmware works!

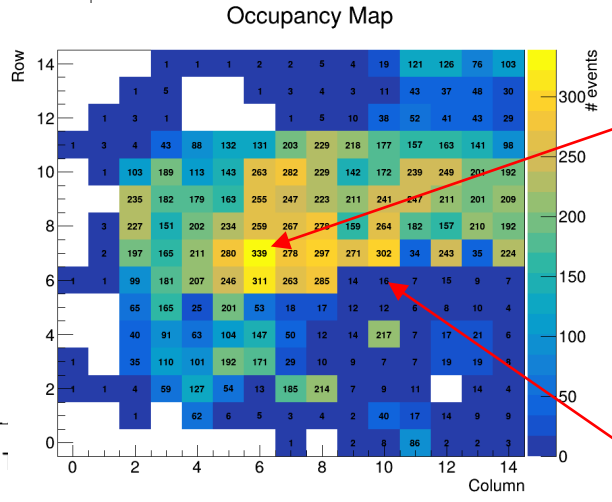
ToA Distribution

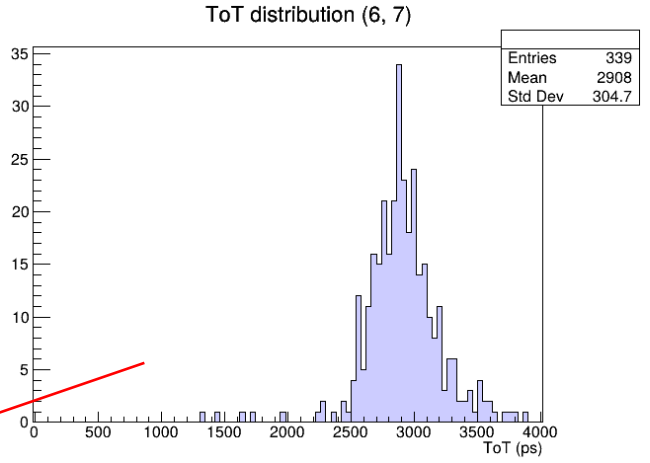


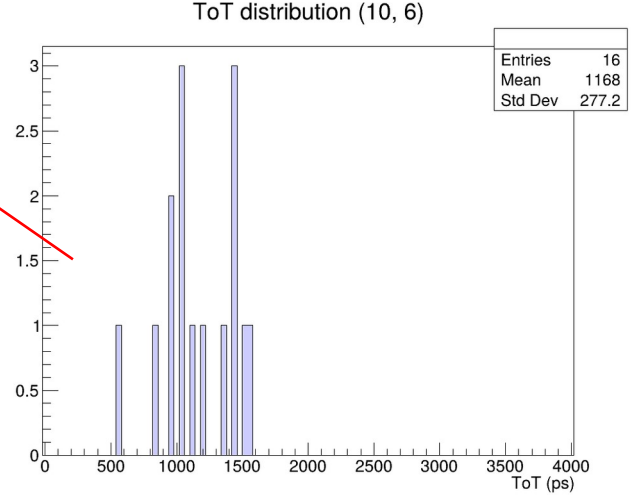
Distribution seems relatively flat, but more statistics is required.

ToT distributions



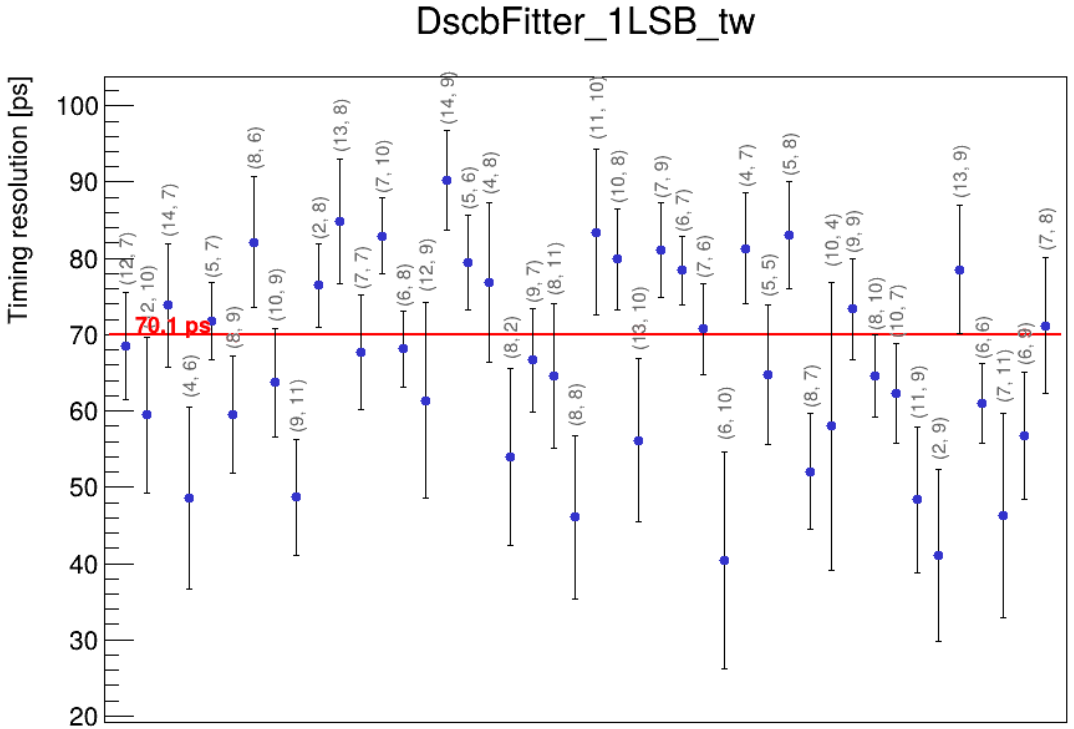




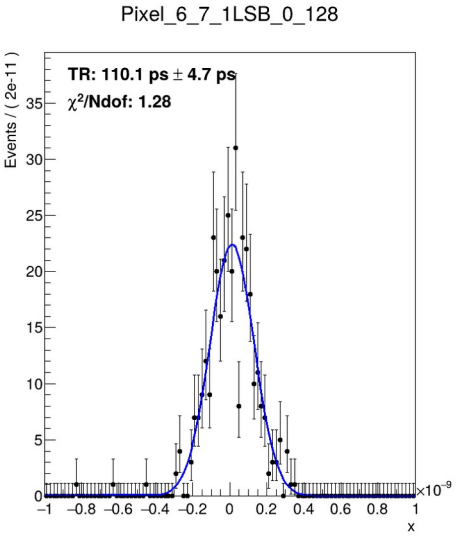


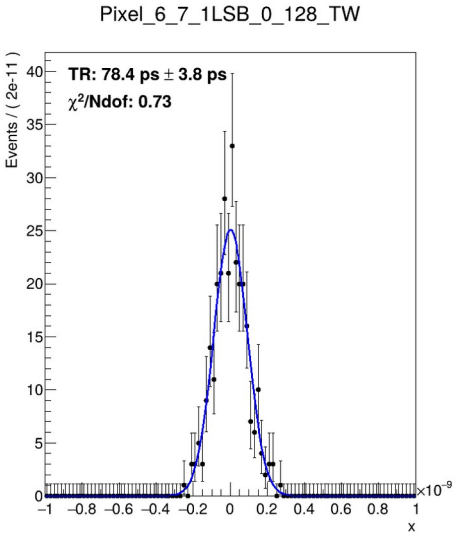
Double peak observed with ToT distribution. This seems to be related to disconnected pixels.

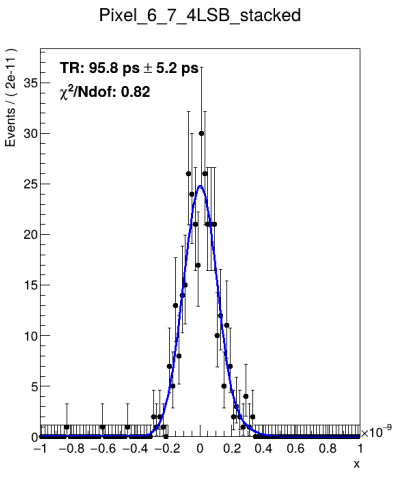
Timing resolution

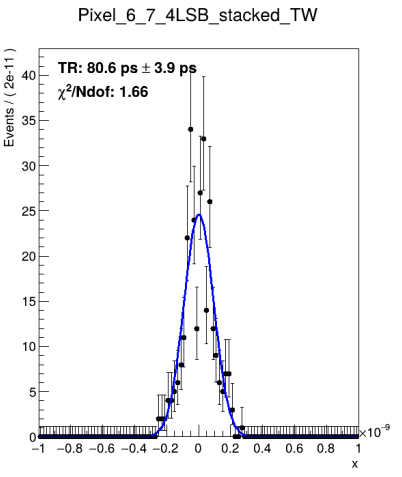


No meaningful results yet as statistics is too low.

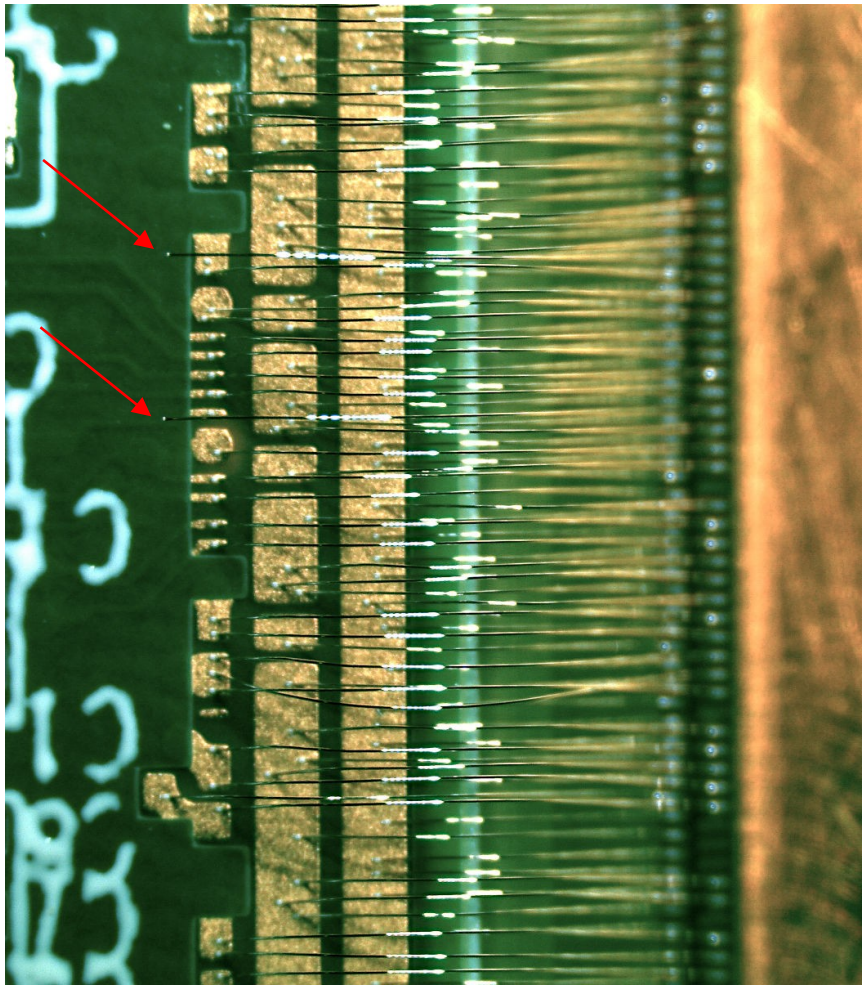


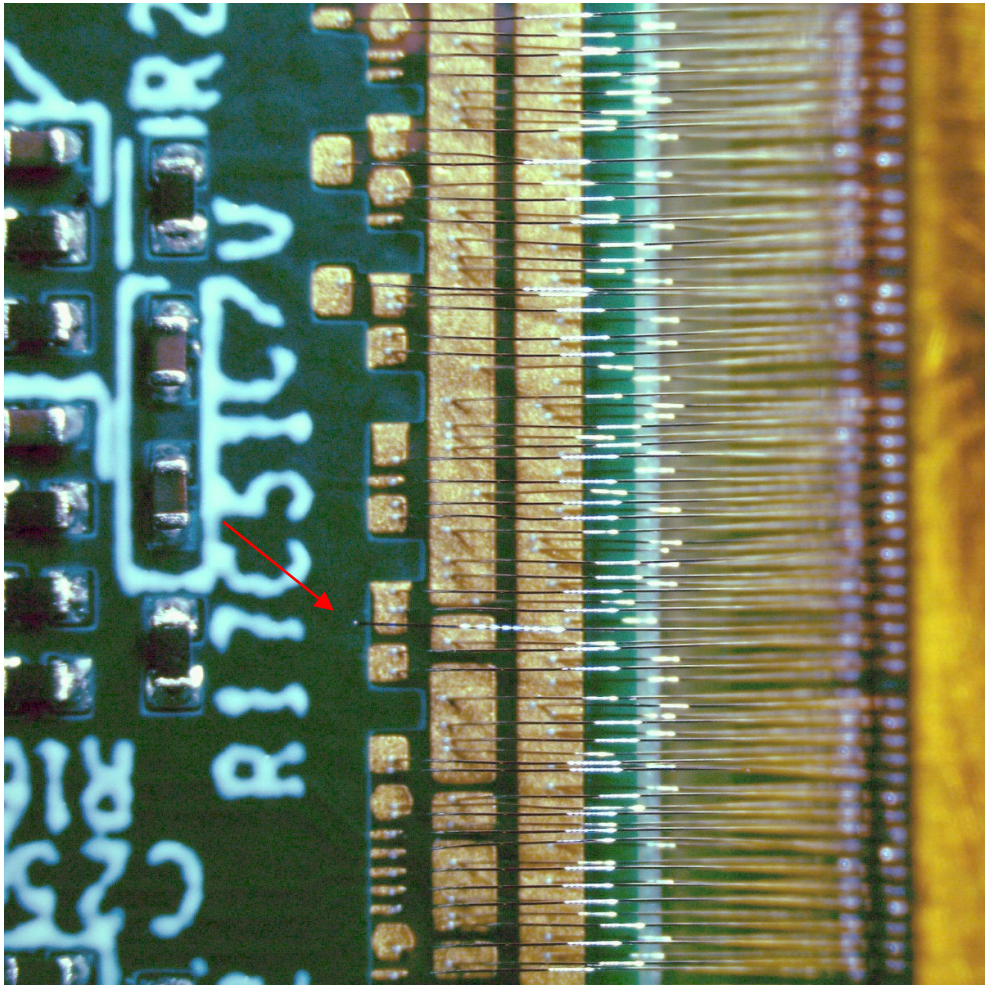




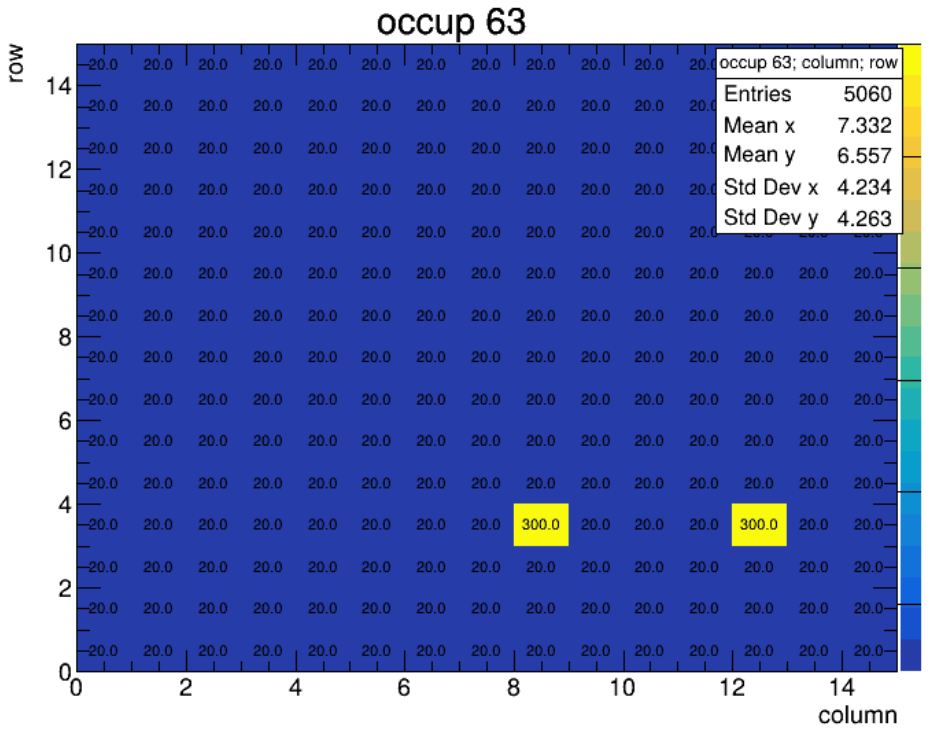


Disconnected bond wires

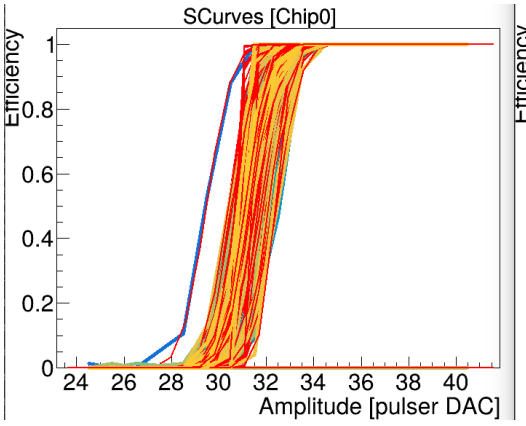


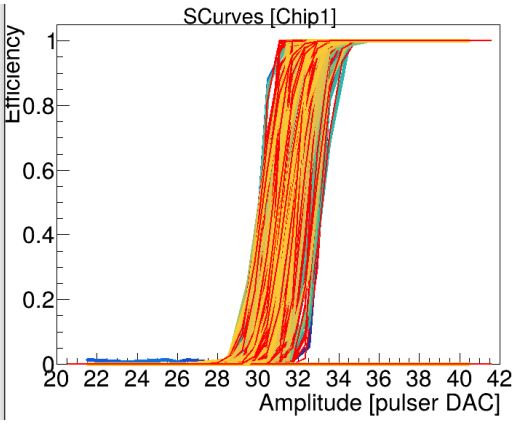


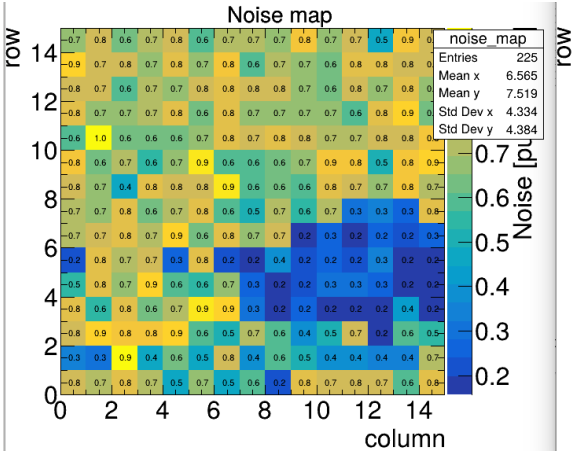
Effects of disconnected bond wires?

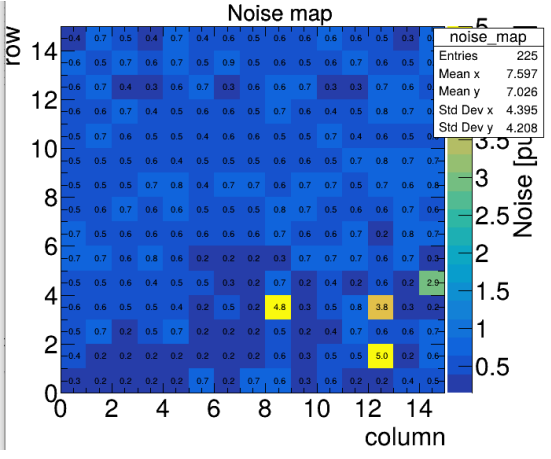


Chip 1 has two defective pixels + multiple noisy ones that need to be masked.

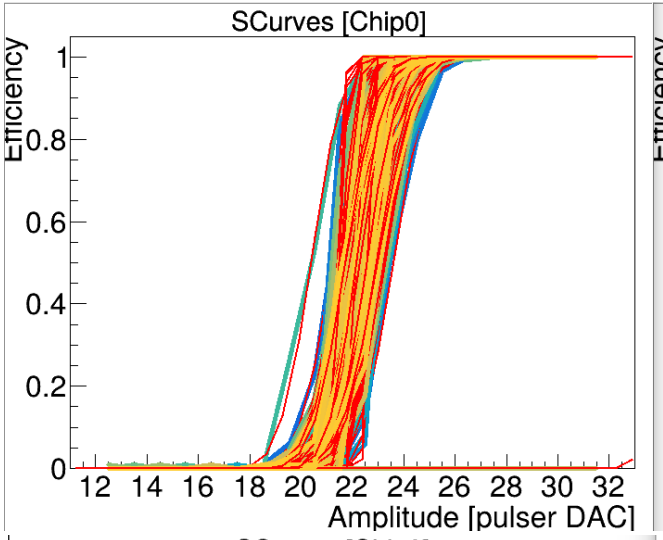


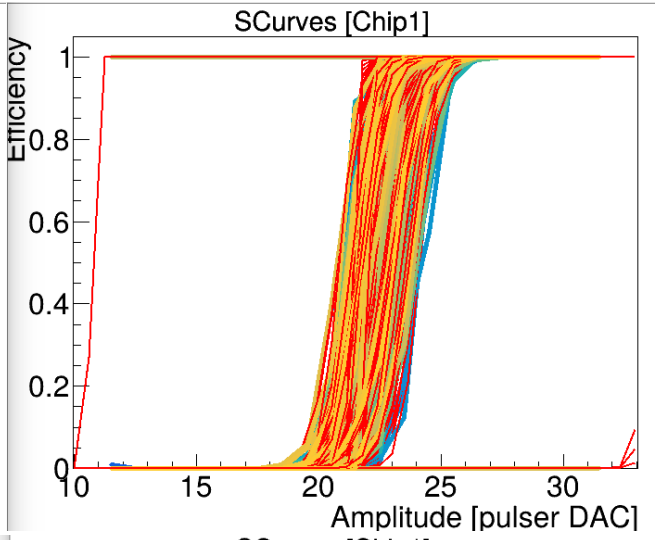


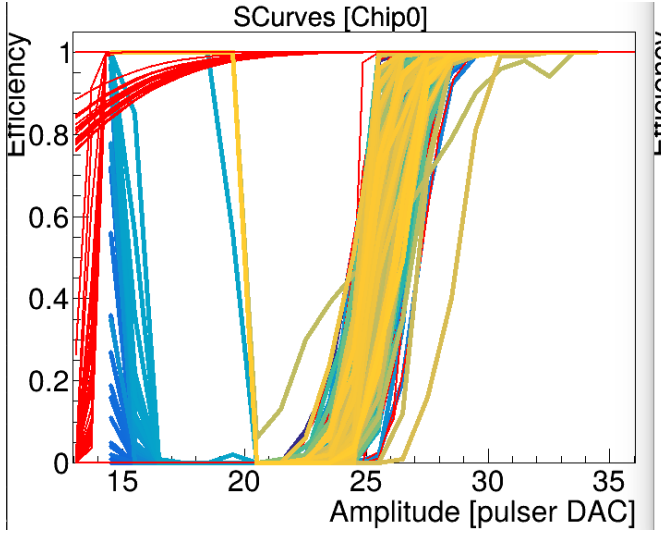


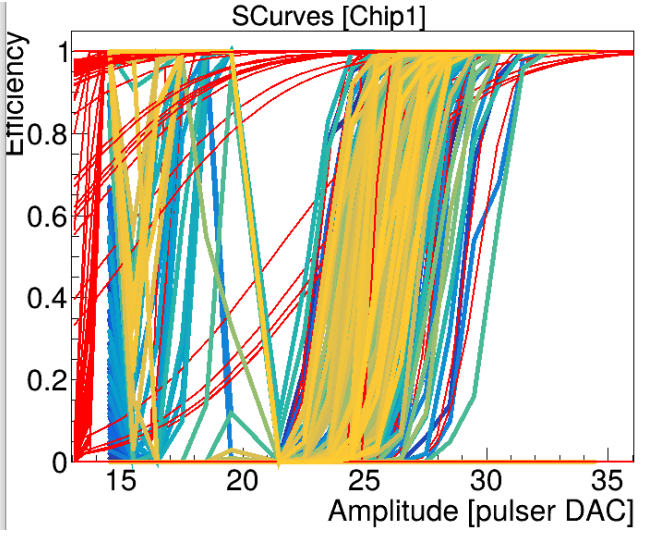


Tuning issues









Was able to tune module to 4.6 fC. Must use 6 fC now for stable operation.

Summary

First timing data from hybrid (Chip 0 only)

- Modified firmware works, can extract clock from FPGA to use as a reference
  - Clock jitter contribution must be calibrated with test board runs (compare timing from interface board / FPGA)
- Some acquisition software tweaks are required to take data for both chips enabled (busy no longer available, data handling)
- Data taking is not stable over long periods of time (possible networking issues)
  - A dedicated network interface for FPGA would help according to previous experience from test beams
- Disconnected wires on module - fix required?
- Tuning issues, was able to tune chips to 4.6 fC now stable only above 6 fC